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(71) Applicant and
(72) Inventor: AUGUSTO, Carlos, J., R., P. [PT/PT]; Rua Sarmento de Beires, N°45, 9A, P-1900 Lisboa (PT).

(74) Agent: VANDERPERRE, Robert; 6-8, avenue de la Charmille, B-1200 Bruxelles (BE).

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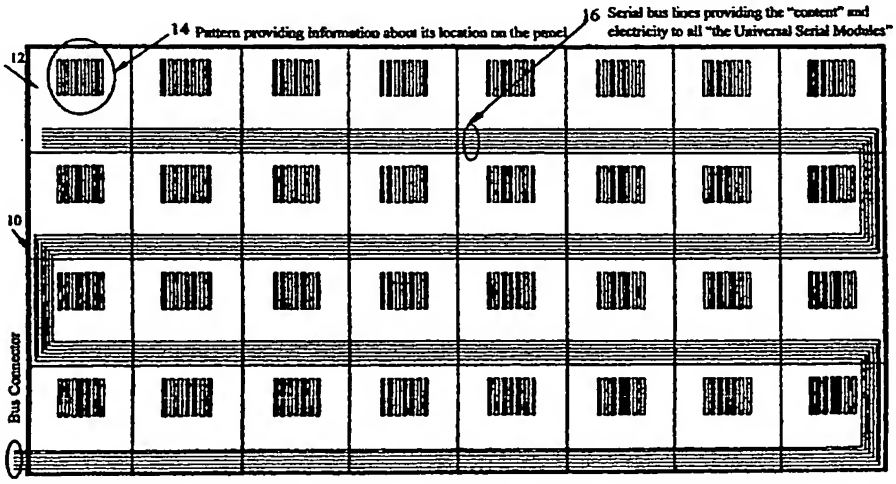
(54) Title: ACTIVE MATRIX FOR FLAT PANEL DISPLAY



(57) Abstract: An Active-Matrix panel for flat panel display, comprising an assembly of universal module units (12) mounted on a common mechanical substrate (10), each module unit being adapted to form a grid of pixels. Module identification means (14) identify the location of each universal module units in the assembly. A serial bus (16) including a number of conducting lines provides data signals and power to the universal module units (12) and contact means are arranged to selectively couple the serial bus to the universal module units for selectively applying data signals and power to each module to selectively activate pixels therein. The pixels are advantageously subdivided into a plurality of sub-pixels (13), whereby a great number of different gray levels or color tones can be produced when bias is selectively applied thereto.

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ACTIVE MATRIX FOR FLAT PANEL DISPLAY

Field of the Invention

The present invention relates generally to Flat Panel Displays (FPDs) and more particularly to reflection-type active-matrix flat panel displays.

Background of the Invention

The replacement of Cathodic Tube Displays (CRTs) by Flat Panel Displays, is of great interest to the consumer electronics industry, and it has been a target pursued by several different technologies, like Plasma Displays, Liquid Crystal Displays (LCDs), Light Emitting Displays (LEDs), Field Emitter Displays (FEDs), etc.

The technical and commercial lead belongs to Liquid Crystal Displays, with "Active-Matrix" addressing. The advantages of "Active-Matrix" technology over passive addressing, are related to the switching speed of each pixel, and independence of refreshing rate of the image being displayed, with display size. In the case of LCDs, it is very straightforward to make the "Active-Matrix" in silicon technology (amorphous or poly-crystalline), due to the compatibility between the materials used.

Historically, "Active-Matrix" Liquid Crystal Displays (AM-FPDs), have been recognized as a superior technology to enable large area, low power, high-resolution displays, in direct view and projection modes. But there are still quite a few problematic areas in need of progress:

1) Higher Resolution (suitable for High Definition Television - HDTV - for example).
2) Better color reproduction,
3) Less light loss to polarizers, color filters, absorption in the back-panel,
4) Improved viewing angle,
5) Break the exponential dependency of production yield, with display area:
    a) Lower the costs by larger yield,
    b) Larger area displays,
6) Integration of the addressing matrix with CMOS for true "System-on-a-Panel" (SoP) technology would increase the functionality through embedded memory and signal processing, reduce the number of components and lower the power consumption, especially for portable/battery-operated products.

Most of these points have been addressed and offered solutions in U.S. Patent No. 5,493,986 in which Carlos J.R.P. Augusto describes a method of providing VLSI-quality crystalline semiconductor substrates for the fabrication of active elements of Active-Matrix

Flat Panel Displays. The present application further elaborates upon those solutions and also offers new ones.

Summary of the Invention

The object of the present invention is to provide a new architecture for the fabrication of Active Matrices usable in flat panel displays (FPDs), especially for the manufacture of large flat panel displays and flat panel displays which include a high density of active elements.

In accordance with the invention, there is provided an active-matrix panel including an assembly of universal modules mounted onto a common mechanical substrate, each universal module including the logic for signal processing to activate the pixels, module identification means to permit auto-identification of each universal module in the assembly, a serial bus comprising conducting lines arranged on the mechanical substrate for providing data signals and power to the universal modules and contact means for selectively applying said data and power signals to each universal module thereby to selectively activate the pixels. Non-volatile memory is advantageously co-integrated with the switching elements.

It is another object of the present invention to provide a high efficiency and low power consuming digital architecture for the pixels. According to the invention, each pixel is subdivided into a plurality of sub-pixels that are selectively activated in a digital format, whereby a great number of gray levels / color tone with maximum intensity can be achieved.

These and other objects, features and advantages will become apparent from the following detailed description, reference being had to the accompanying drawings.

Brief Description of the Drawings

FIG. 1 shows a schematic diagram of the flat panel display architecture in accordance with the present invention;

FIG. 2 shows schematic diagrams representing the architecture of a single digital pixel in accordance with a second aspect of the invention : FIG. 2A to FIG. 2F illustrate different exemplary color tonalities obtained in operation by selective bias applied to the sub-pixels in the geometrical arrangement.

Detailed Description of the Invention

The fabrication of Active Matrices can benefit from VLSI-quality substrates. The fact that a VLSI-quality silicon substrate has a surface defect density many orders of magnitude smaller than a poly-crystalline substrate, which in turn has a similar advantage

over amorphous substrates, is a key advantage for the production of "Active-Matrix" for Flat Panel Displays. The lower defect density, allows for device and circuit scaling in a very similar way to Integrated Circuit (IC) manufacturing, which is something totally out of reach for amorphous or poly-crystalline substrates.

This enables the integration with the Active Matrix, of circuitry that without single-crystal silicon CMOS needs to be provided by additional integrated circuits. Therefore, significant cost savings should be possible from the reduction in the number of process steps, number of components, assembly/mounting of components, etc.

These sharp differences in technical characteristics and manufacturing possibilities of different types of substrates, can be translated into key display properties. The reduction in size and density of defects of substrates, allows for more and smaller electrical devices to be made on those substrates. As a consequence, a larger number of switching elements, each occupying less area, can be put into a display panel. Therefore, more pixels can be packed per unit of area, thus increasing the resolution; and/or more redundant switching elements can be assigned to each pixel, thus enabling higher yields, or larger displays for the same yield.

Because smaller MOS devices have better electrical performances, like larger current drive, operation at lower power supply voltage, higher switching speed, etc., it also mean less power dissipated each time an element switches between the "On-" and "Off-states", or vice-versa. This is particularly relevant for displays in portable products operating on batteries.

Summarizing the advantages brought by VLSI-quality substrates, one has:

- Many different transistor and process architectures are possible,
- Device dimensions scale as in Integrated Circuit manufacturing,
- Device performance (and power consumption) scales like those in Integrated Circuit,
- Circuit design and properties scale like in Integrated Circuit manufacturing,
- High redundancy of switching devices,
- High pixel density, with consequences in display resolution/definition,
- "Active-Matrix" and peripheral circuitry made together on the same substrate,
- Even if there was no technical requirement for an "Active-Matrix", that is, even if the "Light-Valves" could be "addressed" by a "Passive-Matrix", the possibility of integrating all CMOS circuitry onto the back-panel, should be strong enough reason to use single crystal silicon substrates.

With the fabrication of the "Active-Matrix" and other circuit elements on a wafer, before transfer to the final substrate, it is then possible to use a wider choice of substrates.

Among these, are those usually not used in virtue of their intolerance towards high processing temperatures, because they would not be subjected to any high temperature processing.

In U.S. Patent No. 5,493,986 referred to above, there has been described exemplary process flows, which targeted Transmission Displays. A fundamental requisite of this type of display, is the high degree of transparency of the panel onto which the active matrix is fabricated. It is this requisite that leads to process flows, which after the fabrication of the "Active-Matrix", remove the wafer used as substrate for the fabrication of the said "Active-Matrix".

However, for Reflection Displays, the constraint of transparency of the "Active-Matrix" is non-existent. Therefore, there is significantly more freedom in choosing the parameters of the electronic elements of the "Active-Matrix".

For example, it is possible to have a high density of devices in the areas designated for the pixels, if they are fabricated and "interconnected" under the capacitor plate that switches the pixels On and Off.

This only requires that the capacitor plate to be fabricated at a metal level, above all others used for interconnects of the logic and storage devices. In this case, "Large Area Display" does not mean or require "Large Area Electronics", since only the last metallization layer is directly related to the display size. All transistors can be densely packed into a small region. Such scheme clearly bypasses any area penalty associated with the increased functionality of the of the "Active-Matrix", which would not be just an "Active-Matrix" in the conventional meaning of the expression when describing Flat-Panel Displays.

Another advantage of Reflection Displays, is the simplification of the process flow, because there is no need to remove the wafer bulk, because there is no need for a highly transparent substrate.

In the already mentioned U.S. patent, no particular device and/or process architecture was specified for the fabrication of the "Active-Matrix" because, whatever it might be, the Active Matrix would always benefit from VLSI-quality substrates. However, that does not mean that all device/process architectures deliver equal results in terms of overall performance, manufacturability, cost etc.

In order to assure the manufacturability (i.e. high yields) of panel displays with increasing area, two solutions are possible. The first solution is to increase the redundancy in "Active-Matrix" elements. Should one or more fail to work, then there should be other transistors for the same elemental pixel, to make it work properly. For a given pixel size,

this requires increased density of integration, which beyond certain limits, only VLSI-quality substrates make possible.

The second solution, is the modular approach to make bigger displays as teached in U.S. Patent No. 5,493,986. A wafer (of circular shape) is be cut into squares to make a geometrical object (unit) that, when replicated leaves no empty areas between the units. For the purpose, an hexagonal and half-hexagonal shape for the wafer is a better approximation to the circular shape, and therefore, utilize more efficiently the processed area of each wafer. The half-hexagons are needed to make the termination between hexagons so that the outer boundaries become straight lines. This results in less waste in terms of processed silicon from the wafers used to fabricate the "Active Matrix" and other circuitry.

The fabrication of the "Active Matrix" and other circuit elements on a wafer before the transfer to the final substrate, makes it possible to use a wider choice of final substrates. Among these are some that cannot be used during processing, due to materials and temperature incompatibilities.

For Transmission-type displays, a fundamental requisite is the high degree of transparency of the panel onto which the "Active Matrix" is fabricated. It is this requisite that leads to process flows, which after the fabrication of the "Active-Matrix", remove the wafer used as substrate for the processing ("Front-End" and "Back-End" or metallization) of the "Active-Matrix".

However, for Reflection-type displays, the constraint of transparency of the "Active Matrix" is removed. Therefore, there is significantly more freedom in choosing device and process-flow architectures, and also a reduction of the number of process steps, resulting in cost saving.

Fabricating large area FPDs through the assembly or tiling of processed wafers shaped into modules, requires electrical connections between the several modules. A new architecture for the fabrication of AM-FPDs with arbitrary sizes is described herein after with reference to FIG. 1. The architecture according to the invention uses "Universal Smart Modules" (shaped processed wafers) which include very sophisticated CMOS logic (using SD-CMOS technology for example) and large amounts of embedded memory (volatile and/or non-volatile). Therefore, the "Universal Smart Modules" are capable of signal processing and other high performance computations that enable them to perform tasks, like signal compression/decompression, video encoding/decoding, display driving, etc., that with standard FPD technology, are left for circuitry not integrated on the panel.

The Universal Smart Modules are fixed to a common mechanical substrate 10 at locations 12 so as to tile the mechanical substrate. Given their data processing capabilities, rather than interconnecting the modules with metal lines for each column and each row of

all modules to form a giant monolithic "Active Matrix", the interconnects between "Universal Smart Modules" are here performed with a "serial bus" 16 which requires only a few "leads" or metal lines, between the "Universal Smart Modules". Consequently, the interconnects between the "Universal Smart Modules" are extremely simple to be made, precisely because sophisticated and powerful data processing is performed in each "Universal Smart Module".

In operation, each "Universal Smart Module" performs the data processing necessary to display the portion of the image that corresponds to its position relative to the other "Universal Smart Modules" in the large area FPD. The modules are "Universal" because there are no distinctions between them, and any module can be positioned anywhere in the large area FPD. What makes an "Universal Smart Module" to display the "correct" portion of the image, that corresponds to its coordinates on the large area FPD, is the information read from the mechanical substrate, and which was inscribed there by the same method and at the same time when the "serial bus" lines were formed on it.

The interconnects are formed on the final mechanical substrate, before the modules are assembled/mounted. This is especially advantageous to Reflection Displays, because there is no need to assign any area on the front-side of the modules for the inter-module interconnects.

In certain process flows, for the modules to "access" the bus already pre-formed on the mechanical substrate (Back-panel), it is necessary to have "vias" etched through the wafer thickness (actually the device layer, normally would be considerably thinner than a standard wafer), which could be filled with "metal plugs" during the first level of metallization. Since a few "vias" only are needed per "Universal Smart Module", they do not impose serious restrictions regarding the diameter, which can be chosen to facilitate the "deep via" etch process, by providing a manageable aspect ratio. Such deep etch processes ("through-the-wafer") have been demonstrated for micromachining purposes, and stacking of multiple ICs to be mounted on a single package. Other process flows might not require the deep etched "vias" in order to put the modules in electrical contact with the patterns on the mechanical substrate.

Contact pads are provided under each module (with "Auto ID" code). Because they are not in an excessive number, they can have dimensions such that alignment issues are not a problem, and that large area patterning techniques, like screen printing for example, can be used. Techniques like screen printing are capable of printing over extremely large substrates, and are very cost effective.

So, when a large area printing method, like screen printing for example, is used to lay the "serial bus" lines 16 on the large mechanical substrate 10, there is also laid down

some form of code pattern at the location 12 where each module. has to be assembled/mounted. The code pattern can be for instance a pattern of metal pads as shown at 14 in FIG. 1. Like with the "serial bus" lines, the size of the "coding elements" is not a critical issue, and therefore large metal shapes can be formed, without worrying about alignment issues.

The mounting of a module on top of the "serial bus" lines and "coordinate information" makes the "through the wafer vias" to land on top of metal lines. The reading of the coordinate position (Auto Identification ID) can be achieved by testing the current or resistance between sets of "vias". For example, when applying voltage between two of those "vias", if there is a large resistance (basically no current), then it means that there is no metal on the mechanical substrate connecting those "vias". If when applying the voltage between "vias", there is a large current flowing, then it means that both "vias" landed on a metal film that connects them. The verification of the metal pattern under the "Universal Smart Module" with a simple method like this, requires a very basic "self-testing" program that reads that pattern and tells the module its relative position in the FPD, and therefore which portion of the image to display. The pattern with the ID information is specific to the mechanical substrate only. The modules are universal/identical.

It should be emphasized and be very clear that this architecture is meant for Reflection FPDs, and that the "serial bus" connections and ID pattern, are made on the mechanical substrate before the "Universal Smart Modules" are assembled/mounted. The potential alignment problems between the modules and the "serial bus" lines and ID patterns made on the mechanical substrate, are avoided by making those metal lines and patterns large enough and enough separated from each other, so that the modules do not get misaligned.

Sophisticated serial connections with extremely large bandwidths do exist. For example FireWire (IEEE P1394) is now providing 400 Megabits per second. Specifications capable of 800 Mbit/sec are near completion, and specifications for 1.6 Gbit/sec, and 3.2 Gbit/sec are in the definition phase. This serial bus which is also capable of providing power to the peripherals attached to it, has been included in numerous Digital Video Camcorder models from several manufacturers (Sony, Canon, JVC, Panasonic,...) for already a number of years. This bus is also being adopted to connect Digital VCRs (like Digital VHS), Digital TV sets (including HDTV), DVDs, and computers, like the current Apple Macintosh PowerMac G3, and several Sony VAIO models.

In summary, the layout of "Screen Printing Mask" for the mechanical substrate on which the "Universal Smart Modules" will be assembled, should include:

(a) A metal pattern on the substrate under each "Smart Module" (like contact pads for example) for codifying the overall number of modules (and/or size of the panel), and the coordinates of that particular location (the relative position within the panel,

(b) A serial bus comprising a number of conducting lines (left by the Screen Printing process) to carry all data and power signals to every "Universal Smart Module" in the display. The signal processing required to transform the stream of data delivered by the serial bus is performed in each and every "Smart Module", which knowing its relative position in the panel, and the overall panel size, selects the portion of the "Image", it has to display.

With this architecture, there is no need for panel-specific circuitry, either on the mechanical substrate, or in the modules. All modules, being "Smart", are able to figure out all the relevant information and "self-configure" to any display size/shape within the boundaries set by the information contained on the "Auto ID" portion of the layout on the mechanical substrate, and by the bandwidth limitations of the serial bus.

Therefore, it is possible to fabricate "Universal Smart Modules" which can be inserted into any panel of any size or shape, for as long as the panel provides the modules with all the necessary information. With this technology, the cost increases linearly with the number of modules present on a panel (panel size) instead of having an exponential dependence on the area as is the case with conventional "monolithic large area electronics".

FIG. 2 shows a serial bus 16 having a serpentine-like shape, so that all modules are connected using a single masking layer, and without lines crossing over each other. The "Auto ID" patterns 14 are shown by comprising parallel metal stripes that represent binary bits. A solid rectangle is for an existing a metal film. An empty rectangle represents the absence of such a metal film. The modules have "vias" that are supposed to land at opposite extremes of those rectangles. With an applied bias, where there is a metal film (solid rectangle) under "vias", then there will be a current flowing between those "vias". For those "vias" landing on rectangles without metal films (empty rectangles), then there will be no current between them, even when there is an applied bias. Obviously, more sophisticated (complex) Auto ID patterns can be used to "inform" the modules about aspect ratio (1:1, 4:3, 16:9, 2:2, ...) for example.

The universal modules can be fabricated using any advanced technologiy. With 0.18 μm CMOS "Planar Technology" becoming mainstream in 1999, 1GigaBit DRAMs are possible. With this kind of transistor count and fabrication technology, it should very easy to pack a few millions of transistors for an "Active-Matrix" with an yield absolutely comparable to any other kind of IC.

It should again be emphasized that for Reflection Displays, "Large Area Display" does not mean or require "Large Area Electronics", since only the last metallization layer is directly related to the display size. All transistors can be densely packed into a small region, just like in any other IC.

Moreover, with such high number of transistors being available on a single die, a very high transistor redundancy in the "Active-Matrix" should be trivial to fabricate. Therefore, with 0.18 μm CMOS density of integration (or better), not only a highly redundant "Active-Matrix" but also all memory and logic circuitry should be possible to be integrated, effectively making "System on Panel" (SoP) a reality.

In CMOS technology, another device architecture has recently attracted much interest, because of its advantages over standard CMOS technology: the Vertical MOSFET. The advantages of this device architecture are overwhelming when low temperature epitaxy (with the possibility of modulation of dopant and/or heterojunction type and profiles) is employed to define the several regions of the devices. Naturally, to preserve these advantages, the remainder of the processing must also be performed at low temperature.

Along with the device physics advantages, Vertical MOSFETs also enable new process integration architectures which by themselves have many advantages over standard CMOS. These advantages are very compelling from the manufacturability viewpoint, because the "Front-End" process flow for Vertical Integration of Vertical MOSFETs, requires a very reduced number of process steps when compared to standard CMOS.

However, even among Vertical MOSFETs there are significant differences in device structure that result in fundamental differences regarding device physics and integration architectures.

A new CMOS device/process architecture, referred to as Single-Device CMOS (SD-CMOS) has been described in the International Application No. PCT/IB00/00235. The technology described therein has the following features and advantages:

- A single MOSFET behaves as N- or P-type, depending if positive or negative bias is applied (respectively). Only one device needs to be fabricated to make CMOS circuits,
- CMOS Inverters are possible with two identical transistors hardwired to static source voltages; or with just one transistor, having a dynamic source voltage supply,
- The new device architecture and process can be applied to Logic, Memory, Logic with embedded Memory circuits, and also to make "Active-Matrices" for Flat Panel Displays (FPDs)
- Lithography defines the cross-section of the device, i.e. the channel width,
- Channel length (L_{ch}) is defined by low-temperature epitaxy,
- Defect-free junctions (no ion-implantation),

- Footprint is independent of channel length, and therefore operating voltage,
- Resistant against Short Channel Effect (SCE),
- Resistant against Drain Induced Barrier Lowering (DIBL),
- Channel length can be as short as 0.01 μm (10 nm) for room temperature (RT) operation,
- Ultra-low voltage operation (< 0.5 Volt) possible,
- Since SD-CMOS devices can be made with channel lengths of 0.02μm (20nm), it is fairly conservative to expect multi-billion transistor SD-CMOS ICs working at clock frequencies above 200 GHz, "drain current drive" > 1mA/μm, and transconductance (gm) >1000mS/mm for operation at 1Volt,
- Extremely simplified "Front-End" process flow with embedded Ferroelectric memory is possible,
- New layout for "NOR" logic gates, with significant area savings over "NAND" logic gates (the standard in "Planar CMOS"),
- The simultaneous advantages of device performance and process simplification, have unbeatable advantages over any other technology for "System on Chip" (SoC), or "System on Panel" (SoP),
- "System-on-Chip" for fully Digital-RF (no need for analog transistors), also known as "Digital Emitter/Receivers", for RF carrier frequencies up to 100 GHz, are possible.

SD-CMOS is superior to not only standard planar CMOS, but also to previous Vertical MOSFETs, both from device physics and process integration and fabrication flow standpoints.

"Back-panel" microelectronics with SD-CMOS, can be incorporated into any type of displays: Transmission, Reflection, Direct View, Projection, etc. However, there is an advantage to Reflection Displays, in the potential simplification of the process flow, because there is no need for a highly transparent substrate and "Active-Matrix".

Not needing a highly transparent substrate gives complete freedom to distribution of the microelectronic elements in the back-panel as well as their interconnection. For example, it is possible to have a high density of devices under the mirrors of a reflective display. The mirrors can be fabricated at a given metallization level, and therefore be de-coupled not only from the "Front-End" layout, but also from other metallization layers/levels.

This technical characteristic is also very important for another reason, which is the fact that the "integrated circuit size or area" can be de-coupled from the "display size or area". This is true until at least the metallization layer(s) used to fabricated the mirrors. Therefore, the layout and transistor density, can be optimized for performance and yield, without constraints of distributing a transistor for each pixel region.

SD-CMOS, like other Vertical MOSFETs, enables the fabrication of memory cells with 2Fx2F area, which is significantly smaller than the standard 4Fx4F cells of "planar technology" (F is the feature size). This is very relevant to the fabrication of displays, because an "Active-Matrix", in which the matrix elements do not have to be distributed with the individual pixels, can be seen as just a DRAM, whose number of bits is related to the number of pixels of the display.

Further, SD-CMOS technology has another advantage over standard Planar technology and other Vertical MOSFETs in that it enables embedded ferroelectric capacitors to be included from the beginning in the Active Matrix to store the charge that will make the display to retain an image when the power supply is switched off, and this without compromising any factor important to the image quality, like putting some constrains on color filters, light valves, polarizers, etc.

So far, ferroelectric liquid crystals have been used to retain the image on a display, but to obtain this property, other features had to be sacrificed because the ferroelectric light crystals do not possess the highest contrast, switching speed, etc.

The fabrication of ferroelectric capacitors requires the use of certain materials, like BaSrTiO (BST), PbZrTiO (PZT), etc., which for certain stoichiometries exhibit ferroelectric properties. These materials are currently being developed for the Gigabit generation of Integrated Circuit memories.

Once again, by taking advantage of a technology being developed by the Integrated Circuit industry, it will be possible to fabricate displays, where more functionality is included during the fabrication of the "Active Matrix".

In fact, the non-volatile storage of the information could be done through other techniques like Flash Technology, rather than ferroelectric capacitors. The fact that the example given here is based on ferroelectric capacitors, is because they are perceived to be the way of the future, especially for low voltage circuits, and because the process flow can be significantly simpler. However, there should be no loss of generality of the concept, by choosing ferroelectric capacitors to illustrate the concept.

An embedded ferroelectric capacitor can be included from the beginning (not as an afterthought), where the capacitor is a sandwich of epitaxial-metal-barrier/epitaxial-ferroelectric/ epitaxial-metal-barrier.

It has been experimentally demonstrated that epitaxial films significantly enhance the ferroelectric properties by achieving better stoechiometry and crystalline order of the several elements constituting the compound. Examples of such sandwiches epitaxially compatible with silicon, are TiN/BaTiO/TiN and TiN/SrTiO/TiN .

Another aspect of the present invention relates to obtaining the desired color tonality on the display. It is applicable to Transmission Displays, but it is more suitable for Reflection-Displays.

Each "primary color pixel" is subdivided into a plurality of sub-pixels. The number of sub-pixels per primary color pixel, defines the number of different gray levels, or color-tone or color-depth, possible for that "primary color pixel". Different "gray-levels/color-tones" for a "primary color pixel", are defined by different ratios of the numbers of sub-pixels in the "On" and "Off" states. For example, a "primary color pixel" composed of 16x16 sub-pixels, as illustrated in FIG. 2, can display 256 gray levels. The maximum intensity is achieved with the 16x16=256 sub-pixels in the "On-state". FIGs. 2A, 2B and 2C show a pixel architecture with 100 % white pixel, a gray pixel with 25 % of the sub-pixels being black and a gray pixel with 50 % of the sub-pixels being black, respectively. FIG. 2D shows another gray pixel with 50 % of the sub-pixels being black wherein the black sub-pixels are arranged in spaced lines. FIG. 2E shows a gray pixel with 75 % of the sub-pixels being black in a non-symmetric arrangement. FIG. 2F shows a 100 % black pixel.

The digital color-tone architecture according to the invention, which requires a very high ratio of switching elements and respective capacitors per primary color pixel, over the number of "primary color pixels", thus needs very small device geometries in the "Active Matrix", and is only possible with VLSI-quality substrates, preferably with Vertical MOSFETs and, in particular, with SD-CMOS technology.

With this "space-averaging" architecture, wherein the pixels are subdivided into sub-pixels, a sub-pixel failing to work only results is some "infidelity" in the desired gray level (or color tonality), rather than a catastrophic failure of the "primary color pixel". The human eye is not very perceptive of small differences in color tonality, while a white or dark spot on a display is far more likely to be noticed.

The following is an exemplary calculation of the numbers of transistors involved.

"Full color" pixel density of 600 x 600 dpi, translates into primary color pixel area of (42 µm x 42 µm)/3, or about 24 µm x 24 µm. With a color depth of 8 bits, that is 256 levels, for each of these primary color pixels, makes the area of the sub-pixels to be 1.5µmx1.5µm.

This dot (pixel) density is extremely high, and only found in "photo-quality" or "photo-grade" material. This kind of full color pixel resolution, is not necessary for panel sizes typical of TV sets. This kind of resolution is however appropriate for small displays (also called microdisplays), found for example in projection systems, and in small, consumer gadgets, like cell phones for example.

Transmission displays, require the transistor to be much smaller than the pixel itself, and therefore one can easily see that deep sub-micron technology is absolutely needed to obtain such device sizes. But even then, the amount of light absorbed in the panel might not allow for bright enough displays.

This is illustrative of the unique capabilities of using VLSI-quality substrates. At the present moment, amorphous-Si or polycrystalline-Si technologies are now progressing towards 3 μm technology (transistor gate length, not total size) with overall pixel sizes an order of magnitude larger.

"Digital Color Tone architecture" does scale the size of the sub-pixels, with the number of color-tones to be displayed. For high resolution (better than 600 x 600 dpi), and full color display (24 bit), the sub-pixels become 1.5 μm x 1.5 μm.

Actually, the true "digital" nature of this gray-scale/color-tone architecture, can be further exploited. Computers and Digital Television, store the display information in a digital format. Typically, images before being displayed are stored in a frame-buffer, which is a Random Access Memory (RAM). In the frame-buffer, a single frame is stored by assigning to each pixel a logic address, which will have a collection of bits (the color-depth), defining the number of gray-levels or color-tones. With the "Digital Color Tone Architecture" this information is already in the appropriate format to be displayed, and it is not necessary to perform any signal processing, manipulation or format conversion.

The "On/Off" switching of sub-pixels composing an elementary color pixel, can be such that, the "more significant bits" will command the "On/Off" switching of more sub-pixels. For example, for an 8 bit "color-depth", there are 256 (2^8) color tones possible. This color information can be reproduced by an "elementary color pixel" composed of 16 x 16 sub-pixels. The "least significant bit" will switch only 1 sub-pixel. The "second least significant bit" will switch 2 sub-pixels. The "most significant bit" will switch 128 sub-pixels, or an area equivalent. It is advisable to have redundancy, for at least the transistors switching On/Off the most significant bits.

Therefore, for each primary color pixel , the "Active Matrix", has a number of pass-transistors equal to the number of bits (if there is no redundancy) containing the color information (color-depth). The information stored in the frame-buffer and in the "Active Matrix" is the same. Therefore, no extra circuitry (display driver) is required for displaying the content of a "Frame-Buffer"/"Active-Matrix".

For sub-pixel sizes in the order of a micrometer or less, that is, of the order or smaller than the wavelength of visible light, it maybe possible to engineer optical interference effects to reinforce the desired effects.

Because full color images, are formed through a linearly independent combination of the three primary additive colors (R, G, B), then if the three primary color pixels could be positioned on top of each other, rather than side-by-side, the "Digital Color Tone Architecture" would still be applicable, and there would be very important gains in terms of area and/or resolution and/or signal-to-noise ratio. The stacking of the color filters on top of each other is possible given the "right" wavelength-specific color mirror/filters (transparent to the colors that they do not reflect) and the "right" wavelength-specific "Light-Valves" (transparency/opacity controlled separately and independently for each color).

Conventional "Time-Averaging" architectures have big drawbacks. First, they consume more power, because they require frequent switching of the "Light-Valves", and therefore frequent charging and discharging of a capacitor. Second, they require a fast response of the "Light-Valves". Some "Light-Valves" may or may not be able to fulfill this requirement.

The advantages of the "Digital Color Tone Architecture" of the invention can be summarized as follows:

- Fully static,
- Desired tone is achieved by "Space-Averaging" rather than "Time-Averaging",
- Ultra-low power consumption,
- Fully digital (either On or Off) (no calibration or other of requirements typical of analog systems),
- No need for "display-drivers",

Ideal complement to non-volatile memories to produce high-resolution full color displays.

Claims

1. An Active-Matrix panel for flat panel display, said panel comprising a mechanical substrate and an active matrix including switching elements, characterised in that the active matrix is comprised of an assembly of universal module units (12) mounted on a common mechanical substrate (10), each of said module units being adapted to form a grid of pixels, and in that the panel comprises module identification means (14) for identifying the location of each universal module unit in the assembly, a serial bus (16) including a number of conducting lines for providing data signals and power to the universal module units (12), and contact means arranged to selectively couple the serial bus to the universal module units for selectively applying said data signals and power to each module to selectively activate pixels therein.

2. A device as claimed in claim 1, wherein the universal module units are hexagonal and/or half-hexagonal shaped.

3. A device as claimed in either of the preceding claims, wherein the universal module identification means (14) comprise a code pattern positioned underneath each universal module unit.

4. A device as claimed in either of the preceding claims, wherein each pixel (11) is subdivided into a plurality of sub-pixels (13), thereby allowing a great number of different gray levels to be produced when a bias is selectively applied thereto.

5. A device as claimed in either of the preceding claims, wherein a number of pixels (11) are assigned to each primary color and wherein each pixel (11) is subdivided into a plurality of sub-pixels (13).

6. A device as claimed in either of the preceding claims, wherein the arrangements for the different primary colors are stacked on top of each other.

7. A device as claimed in either of the preceding claims, wherein the serial bus (16) is formed in a serpentine-like shape.

8. A device as claimed in either of the preceding claims, wherein the serial bus (16) is formed on the mechanical substrate (10).

9. A device as claimed in either of the preceding claims, wherein non-volatile memory is co-integrated with the switching elements for each pixel.

10. A device as claimed in either of the preceding claims, wherein the active matrix is fabricated using Vertical MOSFET devices.

11. A device as claimed in either of claims 1 to 9, wherein the active matrix is fabricated using SD-CMOS technology.

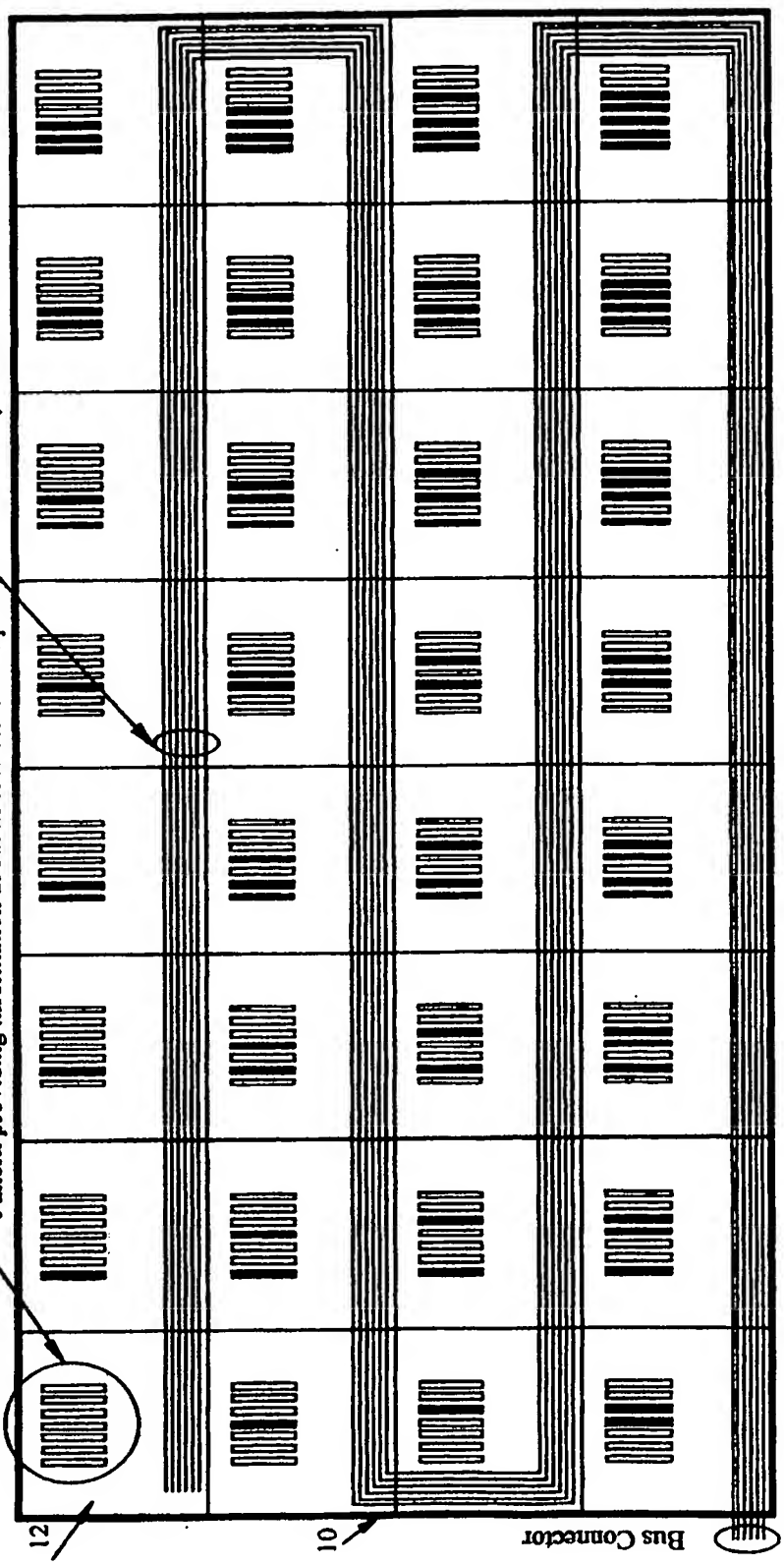
16 Serial bus lines providing the "content" and electricity to all "the Universal Serial Modules"
14 Pattern providing information about its location on the panel
12
10
Bus Connector

Figure 1

Figure 2

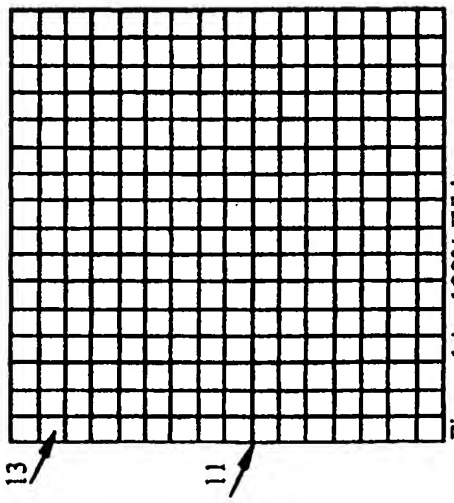

Figure 1A: 100% White

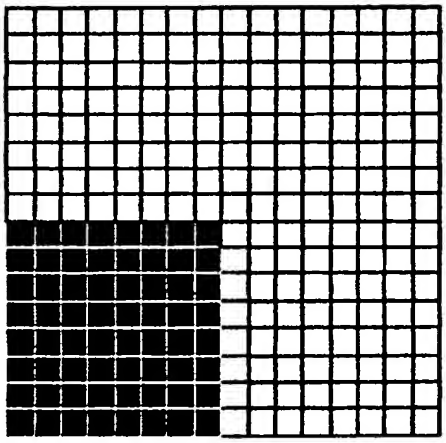

Figure 1B: Gray : 75% White, 25% Black

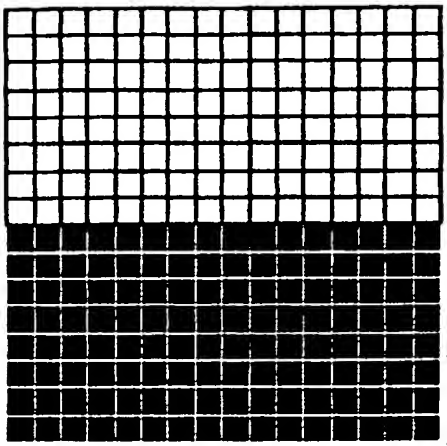

Figure 1C: Gray : 50% White, 50% Black

Figure 1D: Gray: 50% White, 50% Black

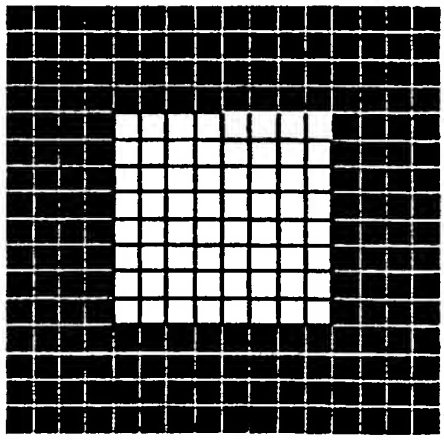

Figure 1E: Gray : 25% White, 75% Black

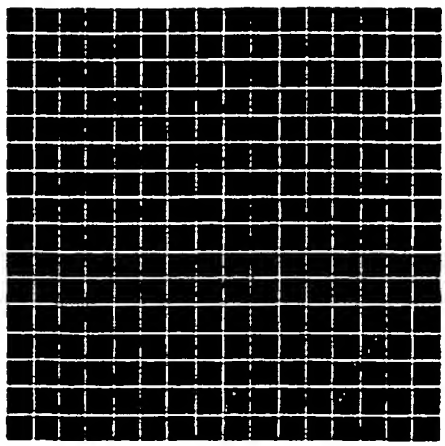

Figure 1F: 100% Black

INTERNATIONAL SEARCH REPORT

Int: onal Application No
PCT/EP 00/05584

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G02F1/1333 G02F1/133 G02F1/1362 G02F1/1368 G09G3/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G02F G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
WPI Data, PAJ, IBM-TDB, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 731 436 A (NISHIDA SHINSUKE) 11 September 1996 (1996-09-11) * sections: [1] - [3] * figures 2-5,9-11,14-16	1,7-9
A	US 5 079 636 A (BRODY THOMAS P) 7 January 1992 (1992-01-07) column 6, line 65 -column 10, line 7 column 12, line 40 -column 14, line 26; figures 1-6	1
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-/—

[X] Further documents are listed in the continuation of box C. [X] Patent family members are listed in annex.

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 September 2000	02/10/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Stang, I

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INTERNATIONAL SEARCH REPORT

Inte onal Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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INTERNATIONAL SEARCH REPORT

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